CLAIMS:

1. A voltage-controlled oscillator comprising a LC tank circuit (L1, L2, VD1, VD2) coupled to a pair of transistors (T2, T3) and crossed-coupled to a pair of emitter follower transistors (T0, T4), each transistor having a collector, an emitter and a base, the voltage controlled oscillator being characterized in that a supply voltage applied to the collectors of the emitter follower transistors (T0, T4) is substantially different from a supply voltage applied to the bases of the emitter follower transistors (T0, T4).

2. A voltage controlled oscillator as claimed in claim 1, wherein the LC tank circuit (L1, L2, VD1, VD2) is coupled to the supply voltage via a bipolar transistor connected as a diode (T7) for obtaining a substantially different supply voltages for the bases and collectors of the emitter follower transistors (T0, T4).

3. A pseudo random sequence generator comprising a first sequence generator (R1) and a second sequence generator (R2) driven by a voltage controlled oscillator as claimed in Claim 1, a first output (O1) of the first sequence generator (R1) and a second output (O2) of the second sequence generator (R2) being coupled to a multiplexer (M) driven by an output signal of the voltage controlled oscillator (I) for selecting either a signal outputted by the first sequence generator (R1) or a signal outputted by the second sequence generator (R2), the multiplexer (M) generating at a third output (O3) a binary signal having a bit-rate (2BR) that is substantially double a bit-rate obtained either at the first output (O1) or at the second output (O2),

4. A pseudo random sequence generator as claimed in Claim 3, wherein each of the sequence generators (R1, R2) comprises a closed-chain of flip-flops (FF_1, ..., FF_{n-1}, FF_n) each having a data input (D_1, ..., D_{n-1}, D_n), a clock input (C_1, ..., C_{n-1}, C_n), a preset input (P_1, ..., P_{n-1}, P_n) and an output (Q_1, ..., Q_{n-1}, Q_n), the pseudo random sequence generator further comprising a feedback including a XOR gate having an output coupled to a first of the flip-flops data input (D1) and a pair of inputs coupled to a pair of outputs of the flip-flops (Q_{n-1},Q_n).